Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An analog-to-digital converter with a pipeline architecture for converting an analog input signal into a digital output signal with a predefined resolution, ~~wherein~~ the converter ~~includes~~ comprising a plurality of stages, each stage having means for converting an analog local signal into a digital local signal with a local resolution lower than said predefined resolution, means for determining an analog residue indicative of a quantization error of the means for converting, and means for amplifying the analog residue by an inter-stage gain corresponding to the local resolution to generate the analog local signal for a next stage; and

means for combining the digital local signals of all the stages into the digital output signal, weighting each digital local signal according to a digital weight depending on the corresponding inter-stage gain, the means for combining includes, for at least one of the stages, means for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain, and means for controlling the digital weight according to the digital correction signal.

2. (Original) The converter of claim 1 wherein the means for estimating includes means for inputting a digital test signal into the at least one stage and means for deriving the digital correction signal from the digital test signal and the digital local signals of the next stages.

3. (Original) The converter of claim 2 wherein the digital test signal and the analog input signal are non-correlated, and the means for deriving the digital correction signal

includes means for correlating the digital test signal with the digital local signals of the next stages.

4. (Original) The converter of claim 3 wherein the digital test signal is pseudo-random.

5. (Original) The converter of claim 4 wherein the means for inputting the digital test signal includes a pseudo-random generator for generating the digital test signal, means for converting the digital test signal into a corresponding analog test signal, and means for adding the analog test signal to the analog local signal.

6. (Original) The converter of claim 5 wherein the means for correlating includes means for calculating a first digital signal multiplying the digital local signal by the digital weight, means for calculating a second digital signal multiplying the digital local signal by the digital weight and the digital correction signal, means for calculating the digital output signal summing the first digital signal, the second digital signal and the digital local signals of the next stages, and means for calculating the digital correction signal from the digital test signal and the digital output signal.

7. (Original) The converter of claim 5 wherein the means for calculating the digital correction signal includes means for calculating a digital residual difference approximating a correlation between the digital test signal and the digital output signal, means for scaling down the digital residual difference, and an integrator for converging towards the digital correction signal according to the digital residual difference.

8. (Original) The converter of claim 7 wherein the means for calculating the digital residual difference includes a multiplier for calculating a third digital signal multiplying the digital test signal by the digital output signal and a digital filter for calculating the digital residual difference from the third digital signal.

9. (Original) The converter of claim 1 wherein the at least one stage consists of a sub-set of consecutive stages starting from a first stage.

10. (Currently Amended) A method of converting an analog input signal into a digital output signal with a predefined resolution using an analog-to-digital converter having a pipeline architecture including a plurality of stages, wherein for each stage the method includes the steps of:

converting an analog local signal into a digital local signal with a local resolution lower than said predefined resolution,

determining an analog residue indicative of a quantization error of the ~~means for converting~~ stage, and

amplifying the analog residue by an inter-stage gain corresponding to the local resolution to generate the analog local signal for a next stage,

and wherein the method further includes the step of:

combining the digital local signals of all the stages into the digital output signal, weighting each digital local signal according to a digital weight depending on the corresponding inter-stage gain, and

for at least one of the stages:

dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain, and

controlling the digital weight according to the digital correction signal.

11. (Original) An analog-to-digital converter, comprising:

a plurality of converter stages comprising a first stage and subsequent stages arranged in a pipeline architecture for converting an analog input signal into a digital output signal with a predefined resolution, each subsequent stage comprising a circuit for amplifying an analog residue by an inter-stage gain corresponding to a local resolution to generate an analog local signal for a next subsequent stage; and

a combining circuit for combining digital local output signals of all the stages into the digital output signal, the combining stage configured to weight each digital local output signal according to a digital weight depending on the corresponding inter-stage gain, and for at least one of the stages a circuit for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain and a circuit for controlling the digital weight according to the digital correction signal.

12. (Original) The converter of claim 11, further comprising an estimation circuit for inputting an digital test signal into the at least one stage and a circuit for deriving the digital correction signal from the digital test signal and the digital local signals of the next subsequent stages.

13. (Original) An analog-to-digital converter, comprising:

a plurality of stages arranged in a pipeline architecture for converting an analog input signal into a digital output signal with a predefined resolution, the plurality of stages including a first stage configured to receive the analog input signal, each of the plurality of stages configured to output a local digital signal; and

a combining circuit configured to combine the local digital signals of all the stages into a digital output signal that weights each local digital signal according to a digital weight depending on a corresponding inter-stage gain, the combining circuit including, for at least one of the stages, a circuit for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain and a circuit for controlling the digital weight according to the digital correction signal.

14. (Original) The converter of claim 13, wherein the combining circuit comprises a digital test signal generator for inserting a test signal into at least the first stage, an amplifier having an input coupled to an output of the first stage and an output coupled to an adder; a second amplifier having an input coupled to the first stage and having an output coupled to a circuit for controlling the digital weight and having an output coupled to the adder, the adder

having an input coupled to an output of the shifter and an output coupled to an output of the converter and to an input of a circuit for correlating the digital test signal with local digital signals of the stages that have an output coupled to the circuit for controlling the digital weight.

15. (Original) The converter of claim 13, further comprising a shifter configured to receive the local digital signals from the plurality of stages.

16. (New) An analog-to-digital converter with a pipeline architecture for converting an analog input signal into a digital output signal with a predefined resolution, the converter comprising a plurality of stages, each stage having means for converting an analog local signal into a digital local signal with a local resolution lower than the predefined resolution, means for determining an analog residue indicative of a quantization error of the means for converting, and means for amplifying the analog residue by an inter-stage gain corresponding to the local resolution to generate the analog local signal for a next stage; and

means for combining the digital local signals of all the stages into the digital output signal, weighting each digital local signal according to a digital weight depending on the corresponding inter-stage gain, the means for combining include, for at least one of the stages, means for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain, and means for controlling the digital weight according to the digital correction signal, wherein the means for estimating include means for inputting a digital test signal into the at least one stage and means for deriving the digital correction signal from the digital test signal and the digital local signals of the next stages.

17. (New) The converter of claim 16 wherein the digital test signal and the analog input signal are non-correlated, and the means for deriving the digital correction signal include means for correlating the digital test signal with the digital local signals of the next stages.

18. (New) The converter of claim 17 wherein the digital test signal is pseudo-random.

19. (New) The converter of claim 18 wherein the means for inputting the digital test signal include a pseudo-random generator for generating the digital test signal, means for converting the digital test signal into a corresponding analog test signal, and means for adding the analog test signal to the analog local signal.

20. (New) The converter of claim 19 wherein the means for correlating include means for calculating a first digital signal multiplying the digital local signal by the digital weight, means for calculating a second digital signal multiplying the digital local signal by the digital weight and the digital correction signal, means for calculating the digital output signal summing the first digital signal, the second digital signal, and the digital local signals of the next stages, and means for calculating the digital correction signal from the digital test signal and the digital output signal.

21. (New) The converter of claim 19 wherein the means for calculating the digital correction signal include means for calculating a digital residual difference approximating a correlation between the digital test signal and the digital output signal, means for scaling down the digital residual difference, and an integrator for converging towards the digital correction signal according to the digital residual difference.

22. (New) The converter of claim 21 wherein the means for calculating the digital residual difference include a multiplier for calculating a third digital signal multiplying the digital test signal by the digital output signal and a digital filter for calculating the digital residual difference from the third digital signal.

23. (New) The converter of claim 16 wherein the at least one stage consists of a sub-set of consecutive stages starting from a first stage.

24. (New) An analog-to-digital converter, comprising:

a plurality of stages arranged in a pipeline architecture for converting an analog input signal into a digital output signal with a predefined resolution, the plurality of stages including a first stage configured to receive the analog input signal, each of the plurality of stages configured to output a local digital signal; and

a combining circuit configured to combine the local digital signals of all the stages into a digital output signal that weights each local digital signal according to a digital weight depending on a corresponding inter-stage gain, the combining circuit including, for at least one of the stages, a circuit for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain and a circuit for controlling the digital weight according to the digital correction signal, wherein the combining circuit comprises a digital test signal generator for inserting a test signal into at least the first stage, an amplifier having an input coupled to an output of the first stage and an output coupled to an adder; a second amplifier having an input coupled to the first stage and having an output coupled to a circuit for controlling the digital weight and having an output coupled to the adder, the adder having an input coupled to an output of the shifter and an output coupled to an output of the converter and to an input of a circuit for correlating the digital test signal with local digital signals of the stages that have an output coupled to the circuit for controlling the digital weight.

25. (New) The converter of claim 24, further comprising a shifter configured to receive the local digital signals from the plurality of stages.

26. (New) A circuit for combining output signals from a plurality of converter stages, comprising:

a combining circuit configured to combine local digital signals generated by each stage, weighting each local digital signal according to a digital weight depending on a corresponding inter-stage gain, the combining circuit including, for at least one of the stages, a circuit for dynamically estimating a digital correction signal indicative of an analog error of the

corresponding inter-stage gain and a circuit for controlling the digital weight according to the digital correction signal.

27. (New) The circuit of claim 26, wherein the combining circuit comprises a digital test signal generator for inputting a digital test signal into the at least one stage and a circuit for deriving the digital correction signal from the digital test signal and the digital local signals of subsequent stages.

28. (New) The circuit of claim 26, wherein the combining circuit comprises a digital test signal generator for inserting a test signal into at least the first stage, an amplifier having an input coupled to an output of the first stage and an output coupled to an adder; a second amplifier having an input coupled to the first stage and having an output coupled to a circuit for controlling the digital weight and having an output coupled to the adder, the adder having an input coupled to an output of the combining circuit and an output coupled to an output of the converter and to an input of a circuit for correlating the digital test signal with local digital signals of the stages that have an output coupled to the circuit for controlling the digital weight.

29. (New) A method of converting an analog input signal into a digital output signal with a predefined resolution using a plurality of converter stages, each stage generating a local digital output signal, the method comprising:

combining the local digital output signals of each stage into a digital output signal, weighting each local digital output signal according to a digital weight depending on a corresponding inter-stage gain, and

for at least one of the stages:

dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain, and

controlling the digital weight according to the digital correction signal.

30. (New) The method of claim 29, wherein each converter stage is configured to generate the local digital output signal in accordance with the following steps:

converting an analog local signal into a local digital output signal with a local resolution lower than the predefined resolution;

determining an analog residue indicative of a quantization error of the stage; and

amplifying the analog residue by the inter-stage gain corresponding to the local resolution to generate the analog local signal for a next stage.

31. (New) The method of claim 30, further comprising inputting a digital test signal into at least a first stage and deriving the digital correction signal from the digital test signal and the local digital output signals of the next subsequent stages.